Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A circuit comprising:

a first transistor, coupled between a first node and a first supply voltage, having a control electrode coupled to an input node of the circuit;

a second transistor coupled between a second supply voltage and the first node;

a third transistor, coupled between a second node and the first supply voltage, having a control electrode coupled to the input node of the circuit;

a fourth transistor, coupled between the second supply voltage and the second node, having a control electrode coupled to the input node of the circuit;

a fifth transistor, coupled between a third node and the first supply voltage, having a control electrode coupled to the second node;

a sixth transistor, coupled between the second supply voltage and the third node, having a control electrode coupled to the first node, wherein the third node is coupled to a control electrode of the second transistor; and

a seventh transistor, coupled between a fourth node and the first node, having a control electrode coupled to the third node.

[c2] The circuit of claim 1 further comprising:
a ninth transistor, coupled between the fourth node and the second supply voltage, having a control electrode coupled to fifth node; and
a logic gate having inputs coupled to an output node of the circuit and a mode control bit, and an output of the logic gate is coupled to the fifth node.

[c3] The circuit of claim 1 further comprising:
an eighth transistor, coupled between the first node and a fifth node, having a control electrode coupled to the input node of the circuit.

[c4] The circuit of claim 1 further comprising:
an eighth transistor, coupled between the first node and a fifth node, having a control electrode coupled to the input node of the circuit;
a ninth transistor, coupled between the fifth node and the first supply voltage, having a control electrode coupled to a sixth node; and
a logic gate having inputs coupled to an output node of the circuit and a mode control bit, and an output of the logic gate is coupled to the sixth node.

[c5] The circuit of claim 2 wherein when the mode control bit is in a first state, the circuit is in a standard buffer mode,

and when the mode control bit is in a second state, the circuit is in a Schmitt trigger mode, and the ninth transistor may be on when the mode control bit is in the first or the second state.

[c6] The circuit of claim 4 wherein when the mode control bit is in a first state, the circuit is in a standard buffer mode, and when the mode control bit is in a second state, the circuit is in a Schmitt trigger mode, and the ninth transistor may be on when the mode control bit is in the first or the second state.

[c7] The circuit of claim 1 wherein a signal at an output node of the circuit is inverted with respect to a signal at the first node.

[c8] A programmable logic integrated circuit comprising a circuit as recited in claim 1.

[c9] An electronic system comprising a circuit as recited in claim 1.

[c10] The circuit of claim 1 further comprising:
an eighth transistor, coupled between the second supply voltage and the supply voltage, having a control electrode coupled to the second node.

[c11] The circuit of claim 10 wherein the eighth transistor is

turned off when a mode control bit indicates the circuit is in a standard buffer mode.

[c12] The circuit of claim 2 wherein the mode control bit is stored using at least one of the following RAM, SRAM, flip flop, register, Flash, EEPROM, EPROM, fuse, or anti-fuse.

[c13] The circuit of claim 2 wherein there are a plurality of mode control bits to indicate an operational mode of the circuit.

[c14] A circuit comprising:
a first transistor, coupled between a first node and a first supply voltage, having a control electrode coupled to an input node of the circuit;
a second transistor coupled between a second supply voltage and the first node;
a third transistor, coupled between a second node and the first supply voltage, having a control electrode coupled to the input node of the circuit;
a fourth transistor, coupled between a third supply voltage and the second node, having a control electrode coupled to the input node of the circuit, wherein the third supply voltage is different from the second supply voltage;
a fifth transistor, coupled between a third node and the

first supply voltage, having a control electrode coupled to the second node;
a sixth transistor, coupled between the second supply voltage and the third node, having a control electrode coupled to the first node, wherein the third node is coupled to a control electrode of the second transistor; and
a seventh transistor, coupled between a fourth node and the first node, having a control electrode coupled to the third node.

[c15] A method of operating a programmable logic integrated circuit comprising:
providing an input buffer capable of operating as a standard buffer in a first mode or a Schmitt trigger in a second mode;
configuring a mode bit to control whether the input buffer operates in the first mode or the second mode;
when in the first mode, using a transistor to couple a supply voltage to a first node of the input buffer depending on a input signal to the input buffer; and
when in the second mode, using a transistor to couple the supply voltage to the first node of the input buffer depending on the input signal to the input buffer and an output signal of the input buffer.

[c16] The method of claim 15 wherein when in the first mode, the input buffer has one switching threshold, and when

in the second mode, the input buffer has a two switching thresholds.

[c17] The method of claim 15 wherein the mode bit may be changed dynamically during the operation of the programmable logic integrated circuit.